CLAIMS:

1. A channel set system comprising:

up to N channels, where $N = 2^M$ and $0 \leq M$, which are addressed using channel addresses; and

a maximum of K channel sets , formed from a combination of the channels, where $K = 2^L$ and $0 \leq L \leq M$, each channel set including up to $Y_{KB}*N/K$ channels, $1 \leq Y_{KB} \leq K$, where Y_{KB} is defined individually for each channel set, and the channel addresses of the channels which are combined to form a specific channel set are contained in a channel address area $(Z_{KB}+i) + j*K \mid 0 \leq i \leq Y_{KB}-1,\ 0 \leq j \leq N/K-1\}$ where $Z_{KB}, 0 \leq Z \leq K-Y_{KB}$, is the channel address of the channel having a lowest channel address permissible for the specific channel set.

2. A channel set system as claimed in claim 1, wherein $1 \leq Y_{KB} \leq 2$.

3. A channel set system as claimed in claim 1, further comprising:

2^X channel groups, each of the channel groups having $N/2^X$ channels where $1 \leq X \leq M$, with each channel being allocated to only one channel group, the channel groups being addressed linearly using group addresses 0 ... 2^X-1, the channels in each of the channel groups also being addressed linearly using channel subaddresses 0 ... $N/2^X$-1, the channel address of a specific channel being obtained by placing the respective group address in front of the channel subaddress of the specific channel, the channel subaddresses of the channels which are combined to form a specific channel set being contained in a channel subaddress area $\{ (Z_{KB}+i) -5*K/2^X + j*K/2^X \mid 0 \leq i \leq Y_{KB}-1,\ 0 \leq j \leq N/K-1\}$ where $Z_{KB}, 0 \leq Z_{KB} \leq K-Y_{KB}$, is the channel address of the channel having the lowest channel address permissible for this channel set, and S, $0 \leq S \leq 2^X$-1, is the group address of the associated channel group.

4. A channel set system as claimed in claim 3, wherein $Z_{KB} - S*K/2^X$ is in each case in the form of the channel set address of the associated channel set.

5. A switching device, comprising:

at least one input stage;

at least one switching module having N input channels and N output channels,

at least one output stage; and

at least one channel set system for connecting the switching module to the output stages, the channel set system further comprising:

up to N channels, where $N = 2^M$ and $0 \leq M$, which are addressed using channel addresses; and

a maximum of K channel sets , formed from a combination of the channels, where $K = 2^L$ and $0 \leq L \leq M$, each channel set including up to $Y_{KB}*N/K$ channels, $1 \leq Y_{KB} \leq K$, where Y_{KB} is defined individually for each channel set, and the channel addresses of the channels which are combined to form a specific channel set are contained in a channel address area $(Z_{KB}+i) + j*K \mid 0 \leq i \leq Y_{KB}-1, 0 \leq j \leq N/K-1\}$ where $Z_{KB}, 0 \leq Z \leq K-Y_{KB}$, is the channel address of the channel having a lowest channel address permissible for the specific channel set.

6. A switching device as claimed in claim 5, wherein each of the at least one switching module is connected to the at least one output stage by a separate channel set system.

7. A switching device as claimed in claim 5 wherein the at least one channel set system further comprises:

2^X channel groups, each of the channel groups having $N/2^X$ channels where $1 \leq X \leq M$, with each channel being allocated to only one channel group, the channel groups being addressed linearly using group addresses $0 .. 2^X-1$, the channels in each of the channel groups also being addressed linearly using channel subaddresses $0 .. N/2^X-1$, the channel address of a specific channel being obtained by placing the respective group address in front of the channel subaddress of the specific channel, the channel subaddresses of the channels which are combined to form a specific channel set being contained in a channel subaddress area $\{ (Z_{KB}+i) -5*K/2^X + j*K/2^X \mid 0 \leq i \leq Y_{KB}-1, 0 \leq j \leq N/K-1\}$ where $Z_{KB}, 0 \leq Z_{KB} \leq K-Y_{KB}$, is the channel address of the channel

having the lowest channel address permissible for this channel set, and S, $0 \leq S \leq 2^X-1$, is the group address of the associated channel group; and

wherein, in the case of a switching module which is implemented with two 2^X switching elements each having N input channels and $N/2^X$ output channels, the addresses of the output channels of the switching elements are identical to the channel subaddresses.

8. A switching device as claimed in claim 5, wherein the at least one channel set system further comprises:

2^X channel groups, each of the channel groups having $N/2^X$ channels where $1 \leq X \leq M$, with each channel being allocated to only one channel group, the channel groups being addressed linearly using group addresses 0 .. 2^X-1, the channels in each of the channel groups also being addressed linearly using channel subaddresses 0 .. $N/2^X-1$, the channel address of a specific channel being obtained by placing the respective group address in front of the channel subaddress of the specific channel, the channel subaddresses of the channels which are combined to form a specific channel set being contained in a channel subaddress area $\{ (Z_{KB}+i) \text{-} 5*K/2^X + j*K/2^X \mid 0 \leq i \leq Y_{KB}-1, 0 \leq j \leq N/K-1\}$ where $Z_{KB}, 0 \leq Z_{KB} \leq K-Y_{KB}$, is the channel address of the channel having the lowest channel address permissible for this channel set, and S, $0 \leq S \leq 2^X-1$, is the group address of the associated channel group; and

wherein the value $K/2^X$ and, at least for each channel set which is used, the value Y_{KB} are indicated to the at least one switching module.